UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,938	05/29/2001	Wendell P. Noble	303.330US3	8033

21186 7590 03/26/2007

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
CHEN, JACK S J	
ART UNIT	PAPER NUMBER
2813	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	09/866,938	NOBLE ET AL.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40,41 and 45-76* is/are pending in the application.

4a) Of the above claim(s) *40,41,45-61,63,64,66 and 68-75* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *62,65,67 and 76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 62, 65, 67 and 76 are rejected under 35 U.S.C. 102(e) as being anticipated by Burns, Jr. et al., US/5,990,509.

Re claim 62, Burns, Jr. et al. disclose a method comprises forming a first source/drain layer 215 at a surface of a substrate 235 (fig. 8); forming a second source/drain layer 240 at a surface of an epitaxial layer (fig. 8, also see col. 9, lines 32-41); etching, in a first direction, a plurality of substantially parallel first troughs (i.e., in the wordline direction) in the epitaxial layer (fig. 8); forming first floating gates 265 along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer 260 (fig. 10); forming first control gate regions 275 between opposing first floating gate region (fig. 10), the first control gate regions being separated from the first floating gates by a first intergate dielectric layer 270 (fig. 10); etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs (i.e., bit line direction) in the epitaxial layer (fig. 8); forming second floating gates 265 along sidewall region of the second troughs and separated from the sidewall regions by a second gate dielectric layer 260 (fig. 11); and forming second control gate regions 275 between opposing second floating gates (fig. 11), the second control

gate regions being separated from the second floating gates by a second intergate dielectric layer 270 (fig. 11), see figs. 1-72 and cols. 1-34 for more details.

Re claim 65, Burns, Jr. et al. disclose a method comprises forming a first source/drain layer 215 at a surface of a substrate 235 (fig. 8); forming a second source/drain layer 240 at a surface of an epitaxial layer (fig. 8, also see col. 9, lines 32-41); etching, in a first direction, a plurality of substantially parallel first troughs (i.e., in the wordline direction) in the epitaxial layer (fig. 8); forming first floating gates 265 along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer 260 (fig. 10); forming first control gate regions 275 between opposing first floating gate region (fig. 10), the first control gate regions being separated from the first floating gates by a first intergate dielectric layer 270 (fig. 10); etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs (i.e., bit line direction) in the epitaxial layer (fig. 8); forming second floating gates 265 along sidewall region of the second troughs and separated from the sidewall regions by a second gate dielectric layer 260 (fig. 11); forming a second intergate dielectric layer 270 by thermal growth of silicon dioxide (col. 11, lines 1-6); and forming second control gate regions 275 between opposing second floating gates (fig. 11), the second control gate regions being separated from the second floating gates by the second intergate dielectric layer 270 (fig. 11), see figs. 1-72 and cols. 1-34 for more details.

Re claim 67, Burns, Jr. et al. disclose a method comprises forming a first source/drain layer 215 at a surface of a substrate 235 (fig. 8), wherein the forming of the first source/drain layer 215 includes forming the first source/drain layer at the surface of the substrate 235, wherein the substrate 235 is a bulk semiconductor; forming a second source/drain layer 240 at a surface

of an epitaxial layer (fig. 8, also see col. 9, lines 32-41); etching, in a first direction, a plurality of substantially parallel first troughs (i.e., in the wordline direction) in the epitaxial layer (fig. 8); forming first floating gates 265 along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer 260 (fig. 10); forming first control gate regions 275 between opposing first floating gate region (fig. 10), the first control gate regions being separated from the first floating gates by a first intergate dielectric layer 270 (fig. 10); etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs (i.e., bit line direction) in the epitaxial layer (fig. 8); forming second floating gates 265 along sidewall region of the second troughs and separated from the sidewall regions by a second gate dielectric layer 260 (fig. 11); and forming second control gate regions 275 between opposing second floating gates (fig. 11), the second control gate regions being separated from the second floating gates by a second intergate dielectric layer 270 (fig. 11), see figs. 1-72 and cols. 1-34 for more details.

Re claim 76, Burns, Jr. et al. disclose a method comprises forming a first source/drain layer 215 at a surface of a substrate 235 (fig. 8); forming a second source/drain layer 240 at a surface of an epitaxial layer (fig. 8, also see col. 9, lines 32-41); etching, in a first direction, a plurality of substantially parallel first troughs (i.e., in the wordline direction) in the epitaxial layer (fig. 8); forming a first gate dielectric layer 260 (fig. 10) along sidewall region of the first troughs; forming first floating gates 265 along sidewall regions of the first troughs and separated from the sidewall regions by the first gate dielectric layer 260 (fig. 10); forming first control gate regions 275 between opposing first floating gate region (fig. 10), the first control gate regions being separated from the first floating gates by a first intergate dielectric layer 270 (fig. 10);

etching, in a second direction substantially orthogonal to the first direction, a plurality of substantially parallel second troughs (i.e., bit line direction) in the epitaxial layer (fig. 8); forming a second gate dielectric 260 (fig. 11) along sidewall regions of the second troughs; forming second floating gates 265 along sidewall region of the second troughs and separated from the sidewall regions by the second gate dielectric layer 260 (fig. 11); and forming second control gate regions 275 between opposing second floating gates (fig. 11), the second control gate regions being separated from the second floating gates by a second intergate dielectric layer 270 (fig. 11), see figs. 1-72 and cols. 1-34 for more details.

Response to Arguments

3. Applicant's arguments filed 12/11/06 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., distinct floating gates) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further in this regard, the prior art also shows that the first and second floating gate regions are distinct floating gates (i.e., each floating gate will perform the same function).

Applicant further argues that the prior art shows a continuous gate region is noted. However, the instant claimed invention does preclude the continuous gate region.

With respect to claims 62, 65, 67 and 76, Applicant states that he/she was unable to find the cited portions of Burns, regarding the phrase "forming first floating gates along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer; forming second floating gates along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer" The above claimed features can be found in the prior art (i.e., figs. 10 and 11, etc.). For example, fig. 10 shows forming first floating gates 265 along sidewall regions of the first troughs and separated from the sidewall regions by a first gate dielectric layer 260 (fig. 10); fig. 11 shows forming second floating gates 265 along sidewall regions of the second troughs and separated from the sidewall regions by a second gate dielectric layer 260 (fig. 11).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

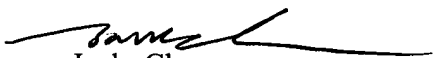
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (8:00am-4:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Jack Chen
Primary Examiner
Art Unit 2813

March 16, 2007